UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.

: 7,096,344 B2

Page 1 of 1

DATED

APPLICATION NO. : 10/695996

DATED

: August 22, 2006

INVENTOR(S)

: Miyamori

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, Item (54), and in Column 1 line 1, the Title is incorrect. Item (54) and Column 1 line 1, should read:

-- EXECUTING PARALLEL PROCESSOR IN DUAL / SINGLE OPERATION INSTRUCTION MODES WITH COPROCESSOR RECEIVING HALT SIGNAL --

Signed and Sealed this

Seventh Day of November, 2006

JON W. DUDAS
Director of the United States Patent and Trademark Office